What is Claimed is:

1. A memory unit with
   - at least two memory areas for storing data,
   - first terminals for accessing data within the memory areas, and
   - second terminals for accessing data within the memory areas,

   characterised by
   - at least two access control means for providing selectively
   - sole addressing and accessing data through one of the terminals, or
   - individual addressing and accessing data through each of the terminals, respectively.

2. The memory unit of claim 1, wherein the first and/or second terminal comprises control ports for receiving control signals for controlling access to the memory areas.

3. The memory unit of claim 1, wherein the first and/or second terminal comprises address ports for receiving addressing signals for addressing data within the memory areas.

4. The memory unit of claim 1, wherein the first and/or second terminal comprises data ports for reading and/or writing data to and/or from the memory areas.

5. The memory unit of claim 1, wherein the access control means provide access to the data areas based on control and/or address signals at said terminals.

6. The memory unit of claim 1, wherein the access control means are state machines, the state machines providing access to the data areas based on states of signals at the first and second terminals.

7. The memory unit of claim 1, wherein the access control means comprise memory registers.

8. The memory unit of claim 3, wherein the address ports provide access to an external address bus.

9. The memory unit of claim 1, wherein the control means provide access to the memory areas by the control ports and the address ports of one of the terminals and provides the data through the data ports of both terminals in case of sole addressing and accessing the data.

10. The memory unit of claim 1, wherein the control means provide access to at least one memory area by the control ports and the address ports of the terminals, respectively, and provides the data through the data ports of the terminals, respectively, in case of individual addressing.

11. The memory unit of claim 10, wherein the control means provide access to at least one memory area by both of the control ports and the address ports of the terminals, and provides the data through the data ports of the terminals, respectively, in case of individual addressing.

12. The memory unit of claim 1, wherein at least two memory areas are provided.

13. The memory unit of claim 1, wherein programming the size of the memory areas is provided through one of the terminals.

14. The memory unit of claim 1, wherein three memory areas are provided.

15. The memory unit of claim 14, wherein two of the three memory areas provide access by the control ports and the address ports of the terminals, respectively, and the data through the data ports of the terminals, respectively.

16. The memory unit of claim 14, wherein the third memory area provide access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of the terminals, respectively.

17. The memory unit of claim 16, wherein the access control means provide prioritised access to the third memory area to one of the terminals.

18. The memory unit of claim 1, wherein one of the terminals provides accessing the data by a central processing unit, and wherein one of the terminals provides accessing the data by a graphics processor.

19. The method unit of claim 1, wherein the bandwidth and/or clocking frequency for the terminals is different.

20. A method for providing access to a memory unit of claim 1 by
- receiving access signals and providing data from memory areas through first terminals, and
- receiving access signals and providing data from memory areas through second terminals,

characterised by
- selectively:
- receiving access signals solely through one terminal and providing data from memory areas through both terminals, or
- receiving access signals and providing data from memory areas through both terminals individually, respectively.

21. A system for providing memory
- with a first processor in communication with a memory unit, and a second processor in communication with the memory unit,

characterised by
- at least two access control means for providing selectively
- sole addressing and accessing data by one of the processors, or
- individually addressing and accessing data by each of the processors, respectively.

22. A module for providing memory to processors, comprising connection terminals providing communication between an electronic circuit and a memory unit of claim 1.

23. A mobile communication device comprising a memory unit of claim 1.